Patent Claims

1. A semiconductor wafer having a multiplicity of semiconductor chips,

- the semiconductor chips having an arrangement of contact areas (1) and test areas (2) which are in each case electrically conductively connected to one another, and
- the contact areas (1) being arranged in a passive first region (5) of the top side of the semiconductor chip (3), the passive first region (5) having no components (6) of an integrated circuit, and
- the test areas (2) being arranged in an active second region (7) of the top side of the semiconductor chip (3), the active second region (7) having components (6) of an integrated circuit.

2. A semiconductor chip having an arrangement of contact areas (1) and test areas (2) which are in each case electrically conductively connected to one another, the contact areas (1) being arranged in a passive, first region (5) of the top side of the semiconductor chip (3), the passive first region (5) having no components (6) of an integrated circuit, the test areas (2) being arranged in an active, second region (7) of the top side of the semiconductor chip (3), the active second region (7) having components (6) of an integrated circuit.

3. The semiconductor wafer or semiconductor chip as claimed in claim 1 or claim 2,
characterized in that
at least one electrically insulating layer (8) comprising, in particular, silicon dioxide and/or silicon nitride is arranged between the components (6) of an integrated circuit and the test areas (2) of the semiconductor chip (3).

4. The semiconductor wafer or semiconductor chip as claimed in one of the preceding claims,
characterized in that
the contact areas (1) and the test areas (2) are electrically conductively connected via a conduction web (4).

5. The semiconductor wafer or semiconductor chip as claimed in claim 4,
characterized in that
through contacts (9) through an insulating layer (8) are arranged in the region of the conduction web (4), the through contacts (9) being connected to interconnects (11) to the electrodes (12) of the components (6) of the integrated circuit.

6. The semiconductor wafer or semiconductor chip as claimed in claim 5,
characterized in that
the interconnects (11) to the electrodes (12) of the components (6) of the integrated circuit comprise copper or a copper alloy.

7. The semiconductor wafer or semiconductor chip as claimed in one of claims 4 to 6,
characterized in that
the contact areas (1) and the test areas (2) at their edges (16) and the conduction web (4) on its top side have a multilayer insulation and passivation layer (15).

8. The semiconductor wafer or semiconductor chip as claimed in claim 7,
characterized in that
the multilayer insulation and passivation layer (15) includes a silicon dioxide layer (17) arranged directly on the edges (16) of the contact areas (1) and of the test areas (2) and on the connecting conduction web

(4).

9. The semiconductor wafer or semiconductor chip as claimed in claim 7 or claim 8,
characterized in that
the multilayer insulation and passivation layer (15) comprises a silicon nitride layer (18) and a polyimide layer (19).

10. The semiconductor wafer or semiconductor chip as claimed in one of claims 4 to 9,
characterized in that
the conduction web (4) is formed in T-shaped fashion, the transverse bar (21) of the T being adapted to the width of the contact areas and having through contacts (9) to interconnects (11), while the longitudinal bar (22) of the T is adapted to the maximum current loading during testing by test tips (23).

11. The semiconductor wafer or semiconductor chip as claimed in one of the preceding claims,
characterized in that
the test areas (2) are adapted in their width (b_P) to the width of the contact areas and have a length (l_P) greater than their width (b_P).

12. An electronic device having a semiconductor chip,
- the semiconductor chip having an arrangement of contact areas (1) and test areas (2) which are in each case electrically conductively connected to one another,
- the contact areas (1) being arranged in a passive, first region (5) of the top side of the semiconductor chip (3), the passive first region (5) having no components (6) of an integrated circuit,
- the test areas (2) being arranged in an active, second region (7) of the top side of the semiconductor chip (3), the active second region (7) having

components (6) of an integrated circuit,
- test areas (2) and contact areas (1) being formed in the same interconnect plane, and
- the length (lp) of the test areas (2) being at least approximately 1.5 times greater than the width (bp) thereof.

13. The electronic device as claimed in claim 12 and also as claimed in one of claims 3 to 11.

14. A method for postprocessing of a semiconductor wafer as claimed in one of claims 1 to 11, the method having the following method steps of:
- providing the semiconductor wafer,
- carrying out a functional test with a test device having test tips,
- marking the defective semiconductor chips.

15. The method as claimed in claim 14,
characterized in that
the step of sealing the test areas is provided.

16. The method as claimed in claim 15,
characterized in that
the test areas are sealed by application of a patterned photoresist layer or soldering resist layer.

17. The method as claimed in one of claims 14 to 16,
characterized in that
the test tips are arranged in offset fashion from test area to test area when carrying out a functional test.